

SEMICONDUCTOR MEMORY AND BURST OPERATION METHOD THEREFOR

Abstract

[0104] The present invention is a PSRAM in which a burst length can be increased without increasing consumed current, and a burst operation method therefor. In operation, column selection lines CSL1 and CSL2 are driven in order during activation of sense amplifiers. This causes bit switches BSW1 - BSW8 to be turned on in units of four bit switches and then 8-bit read data RD is latched from bit line pairs BL1 - BL8 into prefetch/preload latches PFPLL1 - PFPLL8 in units of 4-bits. The 8-bit read data RD is continuously output to a single data I/O bus I/O1 in units of one bit and in order.